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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,725	11/13/2003	Lanc Thomas Holloway	AUS920030181US1	2699

39698 7590 02/16/2007

DUKE W. YEE
YEE & ASSOCIATES, P.C.
P.O. BOX 802333
DALLAS, TX 75380

EXAMINER	
SAVLA, ARPAN P	
ART UNIT	**PAPER NUMBER**
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
2 MONTHS	02/16/2007	PAPER

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/713,725
Filing Date: November 13, 2003
Appellant(s): HOLLOWAY ET AL.

Lisa L.B. Yociss
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed November 13, 2006 appealing from the Office action mailed June 16, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

2002/0095553	Mendelson et al.	7-2002
2001/0001873	Wickeraad et al.	5-2001

Jouppi, Norman P. "Improving Direct-Mapped Cache Performance by the Addition of a Small Fully Associative cache and Prefetch Buffers" IEEE, 1990, pp. 364-373

Tanenbaum, Andrew S. "Structured Computer Organization" Prentice-Hall, Inc., 2nd Edition, 1984, pp. 10-12

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 3, and 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Mendelson et al. (U.S. Patent Application Publication 2002/0095553).

As per claim 1, Mendelson discloses a cache system for a computer system, comprising:

a first cache for storing a first plurality of instructions (paragraph 0003, lines 9-12; paragraph 0028, lines 4-6; paragraph 0033, lines 2-3; Fig. 1C, elements 101_1 - 101_N;

Fig. 3, element 320). *It should be noted that the "filter trace cache (FTC)" is analogous to the "first cache." It should also be noted that "trace" is analogous to "instruction."*

a second cache for storing a second plurality of instructions (paragraph 0028, lines 4-6; Fig. 1C, elements 101_1 - 101_N; Fig. 3, element 330). *It should be noted the "main trace cache (MTC)" is analogous to the "second cache."*

wherein each instruction of the first plurality has an associated counter and wherein when a first instruction of the first plurality is accessed, a first associated counter is incremented (paragraph 0031, lines 10-13; Fig. 3, element 360).

and wherein when the first associated counter reaches a threshold, the first instruction of the first plurality is copied into the second cache (paragraph 0034, lines 15-16). *Again, it should be noted the "main trace cache (MTC)" is analogous to the "second cache."*

As per claim 3, Mendelson discloses the first instruction of the first plurality is accessed from the second cache (paragraph 0035, lines 15-16).

As per claim 6, Mendelson discloses a method of managing cache in a computer system, comprising the steps of:

checking for a first instruction in a first cache, wherein each instruction in the first cache has an associated counter (paragraph 0031, lines 10-11; paragraph 0032, lines 2-3; paragraph 0033, lines 2-3; Fig. 1C, elements 101_1 - 101_N; Fig. 3, elements 320 and

360); *Again, it should be noted that the "filter trace cache (FTC)" is analogous to the "first cache." Again, it should also be noted that "trace" is analogous to "instruction."*

if the first instruction is found in the first cache, incrementing a first associated counter (paragraph 0031, lines 11-13);

comparing a value of the first associated counter to a threshold (paragraph 0034, lines 9-11);

if the first associated counter exceeds the threshold, moving the first instruction from the first cache to a second cache (paragraph 0034, lines 15-16). *Again, it should be noted the "main trace cache (MTC)" is analogous to the "second cache."*

As per claim 7, Mendelson discloses the step of:

accessing the first instruction from the second cache (paragraph 0035, lines 15-17).

Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being obvious over Mendelson in view of Wickeraad et al. (U.S. Patent Application Publication 2001/0001873).

As per claim 2, Mendelson discloses all the limitations of claim 2, except each instruction of the second plurality has an associated counter, and wherein when an instruction of the second plurality is accessed, all other counters of the second plurality are decremented.

Wickeraad discloses each instruction of the second plurality has an associated counter, and wherein when an instruction of the second plurality is accessed, all other counters of the second plurality are decremented (paragraph 0013, lines 2-4 and 8-12). *It should be noted that "memory operand" is analogous to "instruction." It should also be noted that if the "memory operand" is loaded into the cache line it is inherently required the "memory operand" was first accessed from main memory.*

Mendelson and Wickeraad are analogous art because they are from the same field of endeavor, that being cache replacement techniques.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Wickeraad's cache with an associated LRU counter for each cache line within Mendelson's trace cache subsystem.

The motivation for doing so would have been because the algorithm observes both cache hits and cache missed to create correspondence between the cache line selected for replacement and the probability that the cache line will be needed soon, thus, the LRU algorithm tends to be very effective (Wickeraad, paragraph 0012, lines 4-8).

Therefore, it would have been obvious to combine Mendelson and Wickeraad for the benefit of obtaining the invention as specified in claim 2.

As per claim 8, the combination of Mendelson/Wickeraad discloses each instruction of the second cache has an associated counter, and wherein when an

instruction of the second cache is accessed, all other counters of the second cache are decremented (Wickeraad, paragraph 0013, lines 2-4 and 8-12).

Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being obvious over Mendelson in view of Norman P. Jouppi, Improving Direct-Mapped Cache Performance by the Addition of a Small Fully-Associative Cache and Prefetch Buffers, hereafter "Jouppi."

As per claim 5, Mendelson discloses the first cache is an instruction cache (paragraph 0003, lines 9-12; paragraph 0028, lines 4-6; Fig. 1C, elements 101_1 - 101_N; Fig. 3, element 320).

Mendelson does not expressly disclose the second cache is fully associative and follows a least recently used policy.

Jouppi discloses the second cache is fully associative and follows a least recently used policy (pg. 367, section 3.1, lines 4-8).

Mendelson and Jouppi are analogous art because they are from the same field of endeavor, that being cache replacement techniques.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Jouppi's fully associative miss cache which follows a LRU replacement policy within Mendelson's trace cache subsystem.

The motivation for doing so would have been to have a cache that is fully-associative and has LRU replacement, thus eliminating the occurrences of conflict misses (Jouppi, pg. 366, section 3, lines 3-5).

Therefore, it would have been obvious to combine Mendelson and Jouppi for the benefit of obtaining the invention as specified in claim 5.

As per claim 10, the combination of Mendelson/Jouppi discloses the first cache is an instruction cache (Mendelson, paragraph 0003, lines 9-12; paragraph 0028, lines 4-6; Fig. 1C, elements 101_1 - 101_N; Fig. 3, element 320).

Mendelson does not expressly disclose the second cache is fully associative and follows a least recently used policy.

Jouppi discloses the second cache is fully associative and follows a least recently used policy (pg. 367, section 3.1, lines 4-8).

Claims 11-12 are rejected under 35 U.S.C. 103(a) as being obvious over Mendelson in view of Andrew S. Tanenbaum, "Structured Computer Organization, 2nd Edition", hereafter "Tanenbaum."

As per claim 11, Mendelson discloses checking for a first line of data in a first cache, wherein each line of data in the first cache has an associated counter (paragraph 0031, lines 10-11; paragraph 0032, lines 2-3; paragraph 0033, lines 2-3; Fig. 1C, elements 101_1 - 101_N; Fig. 3, elements 320 and 360); *It should be noted that the*

"trace" is analogous to "data." Again, it should also be noted the "filter trace cache (FTC)" is analogous to the "first cache."

if the first line of data is found in the first cache, incrementing a first associated counter (paragraph 0031, lines 11-13);

comparing a value of the first associated counter to a threshold (paragraph 0034, lines 9-11);

if the first associated counter exceeds the threshold, moving the first line of data from the first cache to a second cache (paragraph 0034, lines 15-16). *Again, it should be noted the "main trace cache (MTC)" is analogous to the "second cache."*

Mendelson does not expressly disclose a computer program product in a computer readable medium, comprising:

first instructions for checking for a first line of data in a first cache, wherein each line of data in the first cache has an associated counter;

second instructions for, if the first line of data is found in the first cache, incrementing a first associated counter;

third instructions for comparing a value of the first associated counter to a threshold;

fourth instructions for, if the first associated counter exceeds the threshold, moving the first line of data from the first cache to a second cache.

Tanenbaum discloses that hardware and software are logically equivalent (pg. 11, line 11).

Mendelson and Tanenbaum are analogous art because they are from the same field of endeavor, that being computer hardware.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to follow Tanenbaum's argument and implement Mendelson's trace cache subsystem using instructions on a computer program product in a computer-readable medium having (i.e. implement hardware using software).

The motivation for doing so would have been to optimize such factors as cost, speed, and reliability (Tanenbaum, pg. 11, lines 14-15).

Therefore, it would have been obvious to combine Mendelson and Tanenbaum for the benefit of obtaining the invention as specified in claim 11.

As per claim 12, Mendelson discloses accessing the first instructions from the second cache (paragraph 0035, lines 15-16).

Mendelson does not disclose expressly a computer program, further comprising the step of:

accessing the first instruction from the second cache.

Tanenbaum discloses that hardware and software are logically equivalent (pg. 11, line 11).

Claim 13 is rejected under 35 U.S.C. 103(a) as being obvious over Mendelson in view of Tanenbaum as applied to claim 11 above, and further in view of Wickeraad.

Mendelson/Tanenbaum discloses all the limitations of claim 13 except each instruction of the second cache has an associated counter, and wherein when an instruction of the second cache is accessed, all other counters of the second cache are decremented.

Wickeraad discloses each instruction of the second cache has an associated counter, and wherein when an instruction of the second cache is accessed, all other counters of the second cache are decremented (paragraph 0013, lines 2-4 and 8-12).

Mendelson/Tanenbaum and Wickeraad are analogous art because they are from the same field of endeavor, that being cache replacement techniques.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Wickeraad's cache with an associated LRU counter for each cache line as software within Mendelson/Tanenbaum's software trace cache subsystem.

The motivation for doing so would have been because the algorithm observes both cache hits and cache missed to create correspondence between the cache line selected for replacement and the probability that the cache line will be needed soon, thus, the LRU algorithm tends to be very effective (Wickeraad, paragraph 0012, lines 4-8).

Therefore, it would have been obvious to combine Mendelson/Tanenbaum and Wickeraad for the benefit of obtaining the invention as specified in claim 13.

Claim 15 is rejected under 35 U.S.C. 103(a) as being obvious over Mendelson in view of Tanenbaum as applied to claim 11 above, and further in view of Jouppi.

Mendelson/Tanenbaum discloses the first cache is an instruction cache (paragraph 0003, lines 9-12; paragraph 0028, lines 4-6; Fig. 1C, elements 101_1 - 101_N; Fig. 3, element 320).

Mendelson/Tanenbaum does not expressly disclose the second cache is fully associative and follows a least recently used policy.

Jouppi discloses the second cache is fully associative and follows a least recently used policy (pg. 367, section 3.1, lines 4-8).

Mendelson/Tanenbaum and Jouppi are analogous art because they are from the same field of endeavor, that being cache replacement techniques.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Jouppi's fully associative miss cache which follows a LRU replacement policy as software within Mendelson/Tanenbaum's software trace cache subsystem.

The motivation for doing so would have been to have a cache that is fully-associative and has LRU replacement, thus eliminating the occurrences of conflict misses (Jouppi, pg. 366, section 3, lines 3-5).

Therefore, it would have been obvious to combine Mendelson/Tanenbaum and Jouppi for the benefit of obtaining the invention as specified in claim 15.

(10) Response to Arguments

Response to A.1. (Claim 1)

Appellant argues on page 12 of the Appeal Brief that:

"Unlike Mendelson where traces can stay in the FTC after their counter value reaches a threshold, according to Applicants' claims, the first instruction cannot stay in the first cache after its counter reaches a threshold."

The Examiner respectfully notes that the limitation "the first instruction cannot stay in the first cache after its counter reaches a threshold" is not recited in the language of claim 1.

Appellant argues on page 12 of the Appeal Brief that:

"Because the Examiner does not find explicit reference in Applicants' claim 1 to a time to make a comparison, the Examiner disregards the claim language "when the first associated counter reaches."

The Examiner respectfully disagrees and asserts that the Examiner has fully regarded the broadest reasonable interpretation of all of Appellant's claim language as is detailed below.

Appellant argues on page 13 of the Appeal Brief that:

"Mendelson does not teach copying an instruction the instance the instruction's counter reaches a threshold."

The Examiner notes that there are numerous deficiencies with Appellant's allegation. Firstly, the Examiner respectfully notes that the limitation "copying an instruction the instance the instruction's counter reaches a threshold" is not recited in the language of claim 1.

Secondly, the Examiner asserts that within a computer system, as such is Appellant's invention, although it may seem that to a human that operations are completed "instantaneously" due to the advanced speed of current technology, one of ordinary skill in the art would recognize that it is not physically possible to copy the first instruction the instance the counter reaches a threshold.

All components within a computer system experience a discrete latency (i.e. time delay) during all operations. This is due to engineering limitations as well as inherent laws of physics dealing with propagation delay. No action in the entire universe, not even propagation of electromagnetic radiation, occurs instantaneously. Thus, Appellant's allegation that "the instance the counter reaches a threshold, the first instruction is copied" is in error.

Appellant argues on page 13 of the Appeal Brief that:

"Mendelson does not teach a trace being copied when its value reaches a threshold. In Mendelson, a trace can remain in the FTC with its value well above the threshold. Therefore, Mendelson does not teach when the first associated counter

reaches a threshold, the first instruction of the first plurality is copied into the second cache. Therefore, Mendelson does not anticipate Applicants' claim 1."

The Examiner respectfully disagrees. Insofar as it appears to be clear, it is inherently required that a comparison is made between the first associated counter value and the threshold value. Appellant states that "Applicants' do not claim a specific time to make a comparison" but later states that "The broadest most reasonable interpretation of Applicants' claim 1 is that a comparison is continuous", see Appeal Brief, page 13. However, the Examiner respectfully notes that this language is not recited in claim 1. The Examiner refers Appellant to Mendelson paragraph 0034, lines 12-16 which recites:

> "When a trace is needed to be evicted from the FTC 320, the comparator 380 compares the stored threshold number J to the number of accesses extracted the usage counters $360_N - 360_N$. If the number of access is equal to or higher than the threshold number "J", the trace is moved to the MTC."

As is clearly shown in the cited portion of Mendelson directly above, Mendelson specifies the time at which the comparison is made ("when a trace is needed to be evicted from the FTC (i.e. first cache)"). Mendelson then further specifies that when the number of accesses ("associated counter value") is equal to ("reaches") or greater than the threshold, the trace ("instruction") is moved ("copied") to the MTC ("second cache").

Assuming, *in arguendo*, that the limitation "copying an instruction the instance the instruction's counter reaches a threshold" is in fact recited in the language of Appellants' claim 1 and also that it is in fact physically possible to copy an instruction the instance the instruction's counter reaches a threshold, Mendelson still anticipates claim 1. In

Mendelson, there is no restriction as to when a trace can be evicted. Hence, it is possible for a trace to be evicted at any given time. Take the situation when a trace needs to be evicted at the same instant the number of accesses in the trace's usage counter reaches the threshold number "J". In this situation the comparator compares the stored threshold number "J" to the number of accesses in the trace's usage counter. The number of accesses is equal to the threshold number "J", therefore, the trace is moved to the MTC. Thus, the trace is copied to the MTC the instance the trace's usage counter reaches the threshold number "J." Accordingly, Mendelson sufficiently discloses Appellants' claim 1.

Response to A.2. (Claim 6)

Appellant argues on page 13 of the Appeal Brief that:

"Mendelson teaches each trace having an access counter that counts accesses to the trace since it was inserted into a particular trace cache. See Mendelson, paragraph 0030. In contradistinction, Applicants' claim 6 recites incrementing a counter if an instruction is found in the cache. Finding a trace in a cache and accessing a trace in a cache are not the same."

The Examiner respectfully notes that while finding a trace (i.e. instruction) in a cache and accessing a trace in a cache may not be the exact same actions, the Examiner asserts that accessing a trace in a cache anticipates finding a trace in a cache. This is so because in order to access a trace in cache the trace must be first

found in cache. Thus, any and all accesses of a trace always require the trace first be found.

Appellant argues on page 13 of the Appeal Brief that:

"According to Applicants' claim 6, a counter would be incremented even when an instruction is found in cache, but never accessed."

The Examiner respectfully notes that this limitation is not recited in the language of claim 6. The second limitation in claim 6 merely recites "if the instruction is found in the first cache, incrementing a first associated counter." Thus, Appellants' claim language is not concerned if the instruction is found, but never accessed. Appellants' claim language is only concerned if the instruction is merely found. And as explained directly above, anytime an instruction is accessed it always requires the instruction is found.

Appellant argues on pages 13-14 of the Appeal Brief that:

"Mendelson does not teach checking for an instruction in a cache, and then incrementing a counter if the instruction is found *in the cache. Mendelson teaches counting the number of times an actual access of a trace occurs. Merely finding a trace in the cache does not result in incrementing the counter according to Mendelson. The trace must be accessed.*

Because Mendelson does not teach checking for an instruction in a cache, and then incrementing a counter if the instruction is found in the cache, Mendelson does not anticipate Applicants' claim 6."

The Examiner respectfully disagrees and refers Appellant to Mendelson, paragraph 0032, lines 2-3 which state:

"Every fetch is attempted in both FTC 320 and MTC 330."

As one of ordinary skill in the art would know the term "fetch" describes retrieving an instruction from memory. Therefore, "attempting an instruction fetch in a cache" is equivalent to "checking for an instruction in a cache." Accordingly, Mendelson sufficiently discloses checking for an instruction in a cache.

As detailed in the previous sections of the response to A.2. directly above, the Examiner asserts that accessing an instruction in a cache anticipates finding an instruction in a cache, thus, accessing an instruction always requires finding the instruction. Mendelson discloses if a trace (i.e. instruction) is accessed (and therefore correspondingly found), the associated counter for that trace is incremented (see Mendelson, paragraph 0031, lines 11-13 as cited in the rejection above). Accordingly, Mendelson sufficiently discloses if the instruction is found in the first cache, incrementing a first associated counter.

Response to B.1. (Claim 2)

Appellant argues on page 14 of the Appeal Brief that:

"It is important to note that the second instruction claimed by Applicants is already stored in the second cache when it is accessed."

The Examiner respectfully disagrees and notes that nowhere in the language of claims 1 or 2 does it recite that the second instruction is already stored in the second

cache when it is accessed. The second limitation of claim 1 recites "a second cache for storing a second plurality of instructions." This limitation merely recites storing a second plurality of instructions as an intended use of a second cache. The limitation fails to positively recite that a second plurality of instructions is stored in a second cache, but rather recites that a second cache is capable of storing a second plurality of instructions. Thus, Appellant's allegation that "the second instruction claimed by Applicants is already stored in the second cache when it is accessed" is in error.

Appellant argues on pages 14-15 of the Appeal Brief that:

"Because the combination of Mendelson and Wickraad (sic) does not teach an instruction that is already stored in the cache being accessed, resulting in decrementing the counters of the other instructions that are stored in the cache, the combination does not render Applicants' claim 2 obvious."

The Examiner respectfully notes again that nowhere in the language of claims 1 or 2 does it recite that the second instruction is already stored in the second cache when it is accessed and directs Appellant to the first section of the response to B.1. directly above.

Response to B.2. (Claim 8)

Appellant argues on page 15 of the Appeal Brief that:

"Mendelson does not teach checking for an instruction in a cache, and then incrementing a counter if the instruction is found *in the cache. Mendelson teaches*

counting the number of times an actual access of a trace occurs. Merely finding a trace in the cache does not result in incrementing the counter according to Mendelson. The trace must be accessed.

The combination of Mendelson and Wickraad (sic) does not render Applicants' claim 8 obvious because the combination does not teach or suggest checking for an instruction in a cache, and then incrementing a counter if the instruction is found in the cache in combination with each instruction of the second cache having an associated counter, and wherein when an instruction of the second cache is accessed, all other counters of the second cache are decremented."

The Examiner respectfully disagrees and refers Appellant above to the response to A.2. which details how Mendelson discloses checking for an instruction in a cache, and then incrementing a counter if the instruction is found in the cache as well as the response to B.1. which details how Wickeraad discloses when an instruction of the second cache is accessed, all other counters of the second cache are decremented. Accordingly, the combination of Mendelson and Wickeraad renders Appellants' claim 8 obvious.

Response to C.1. (Claim 5)

Appellant argues on page 16 of the Appeal Brief that:

"The combination of Mendelson and Jouppi does not render Applicants' claim 5 obvious because the combination does not teach the first instruction being copied when the first associated counter reaches a threshold and the first cache being an instruction

cache and the second cache being fully associative and following a least recently used policy."

The Examiner respectfully disagrees refers Appellant above to the response to A.1. which details how Mendelson discloses the first instruction being copied when the first associated counter reaches a threshold. The Examiner also refers Appellant to the rejection of claim 5 above and more specifically to Mendelson, paragraph 0003, lines 9-12 and paragraph 0028 which discloses the first cache is an instruction cache as well Jouppi, pg. 367, section 3.1, lines 4-8 which discloses the second cache is fully associative and follows a least recently used policy. Accordingly, the combination of Mendelson and Jouppi renders Appellants' claim 5 obvious.

Response to C.2. (Claim 10)

Appellant argues on page 16 of the Appeal Brief that:

"Mendelson does not teach checking for an instruction in a cache, and then incrementing a counter if the instruction is found *in the cache. Mendelson teaches counting the number of times an actual access of a trace occurs. Merely finding a trace in the cache does not result in incrementing the counter according to Mendelson. The trace must be accessed.*

The combination of Mendelson and Wickraad (sic) does not render Applicants' claim 8 obvious because the combination does not teach or suggest checking for an instruction in a cache, and then incrementing a counter if the instruction is found in the cache in combination with each instruction of the second cache having

an associated counter, and wherein the first cache is an instruction cache and the second cache is full associative and follows a least recently used policy."

Firstly, the Examiner believes that Appellant mistakenly wrote "The combination of Mendelson and Wickraad (sic) does not render Applicants' claim 8..." and actually meant to write "The combination of Mendelson and Jouppi does not render Applicants' claim 10 obvious..."

Based on this observation, the Examiner respectfully disagrees and refers Appellant above to the response to A.2. which details how Mendelson discloses checking for an instruction in a cache, and then incrementing a counter if the instruction is found in the cache. The Examiner also refers Appellant to the rejection of claim 10 above and more specifically to Mendelson, paragraph 0003, lines 9-12 and paragraph 0028 which discloses the first cache is an instruction cache as well Jouppi, pg. 367, section 3.1, lines 4-8 which discloses the second cache is fully associative and follows a least recently used policy. Accordingly, the combination of Mendelson and Jouppi renders Appellants' claim 10 obvious.

Response to D. (Claims 11 and 12)

Appellant argues on page 17 of the Appeal Brief that:

"Mendelson teaches each trace having an access counter that counts accesses to the trace since it was inserted into a particular trace cache. See Mendelson, paragraph 0030. In contradistinction, Applicants' claim 11 recites incrementing a counter

if an instruction is found in the cache. Finding a trace in a cache and accessing a trace in a cache are not the same."

The Examiner refers Appellant above to the first section of the response to A.2. which details how accessing a trace in cache anticipates finding a trace in cache.

Appellant argues on page 17 of the Appeal Brief that:

"According to Applicants' claim 11, a counter would be incremented even when an instruction is found in cache, but never accessed."

The Examiner refers Appellant above to the second section of the response to A.2. which details how this limitation is not recited in the claim language.

Appellant argues on pages 17 of the Appeal Brief that:

"Mendelson does not teach checking for an instruction in a cache, and then incrementing a counter if the instruction is found *in the cache. Mendelson teaches counting the number of times an actual access of a trace occurs. Merely finding a trace in the cache does not result in incrementing the counter according to Mendelson. The trace must be accessed.*

Because Mendelson does not teach checking for a first line of data in a first cache, wherein each line of data in the first cache has an associated counter; second instructions for, if the first line of data is found in the cache, incrementing a first associated counter, the combination of Mendelson and Tanenbaum does not render Applicants' claim 11 and 12 obvious."

The Examiner respectfully disagrees and refers Appellant above to the third section of the response to A.2. which details how Mendelson discloses checking for a first line of data (i.e. trace) in a first cache, wherein each line of data in the first cache has an associated counter; if the first line of data is found in the cache, incrementing a first associated counter. Accordingly, the combination of Mendelson and Tanenbaum renders Appellants' claims 11 and 12 obvious.

Response to E. (Claim 13)

Appellant argues on page 18 of the Appeal Brief that:

"The combination of Mendelson, Tanenbaum, and Wickeraad does not render Applicants' claim 13 obvious because the combination does not teach checking for a first line of data in a first cache, wherein each line of data in the first cache has an associated counter; second instructions for, if the first line of data is found in the first cache, incrementing a first associated counter, in combination with wherein each line of data of the second cache has an associated counter, and wherein when a line of data of the second cache is accessed, all other counters of the second cache are decremented."

The Examiner respectfully disagrees and refers Appellant above to the response to A.2. which details how Mendelson discloses checking for a first line of data in a first cache, wherein each line of data in the first cache has an associated counter; if the first line of data is found in the first cache, incrementing a first associated counter as well as the response to B.1. which details how Wickeraad discloses each line of data of the

second cache has an associated counter, and wherein when a line of data of the second cache is accessed, all other counters of the second cache are decremented. Accordingly, the combination of Mendelson, Wickeraad, and Tanenbaum renders Appellants' claim 13 obvious.

Response to F. (Claim 15)

Appellant argues on page 19 of the Appeal Brief that:

"The combination of Mendelson, Tanenbaum, and Jouppi does not render Applicants' claim 15 obvious because the combination does not teach checking for a first line of data in a first cache, wherein each line of data in the first cache has an associated counter; second instructions for, if the first line of data is found in the first cache, incrementing a first associated counter, in combination with wherein the first cache is an instruction cache and the second cache is fully associative and follows a least recently used policy."

The Examiner respectfully disagrees and refers Appellant above to the response to A.2. which details how Mendelson teach checking for a first line of data in a first cache, wherein each line of data in the first cache has an associated counter; if the first line of data is found in the first cache, incrementing a first associated counter. The Examiner also refers Appellant to the rejection of claim 15 above and more specifically to Mendelson, paragraph 0003, lines 9-12 and paragraph 0028 which discloses the first cache is an instruction cache as well Jouppi, pg. 367, section 3.1, lines 4-8 which discloses the second cache is fully associative and follows a least recently used policy.

Accordingly, the combination of Mendelson, Tanenbaum, and Jouppi renders Appellants' claim 15 obvious.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Arpan Savla

Conferees:

Sanjiv Shah

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Lynne H. Browne

Lynne H. Browne
Appeal Specialist, TQAS
Technology Center 2100